THE INVENTION CLAIMED IS:

1. A method of forming a device comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming a sidewall spacer on the semiconductor substrate adjacent the gate and the gate dielectric;

forming a thickening layer by selective epitaxial growth on the semiconductor substrate adjacent the sidewall spacer;

forming raised source/drain dopant implanted regions in at least a portion of the thickening layer;

forming silicide layers in at least a portion of the raised source/drain dopant implanted regions to form source/drain regions, beneath the silicide layers, that are enriched with dopant from the silicide layers;

depositing a dielectric layer over the silicide layers; and

forming contacts in the dielectric layer to the silicide layers.

2. The method as claimed in claim 1 wherein forming the raised source/drain dopant implanted regions further comprises implanting dopant into the thickening layer and the adjacent top of the semiconductor substrate.

3. The method as claimed in claim 1 wherein forming silicide layers in the raised source/drain dopant implanted regions further comprises:

depositing metallic layers on the raised source/drain dopant implanted regions; and

forming silicide layers by thermal silicidation of the metallic layers into the material of the raised source/drain dopant implanted regions.

4. The method as claimed in claim 1 wherein forming silicide layers in the raised source/drain dopant implanted regions to form source/drain regions therebeneath that are enriched with dopant from the silicide layers further comprises forming source/drain regions that are enriched with a dopant profile that is steeper than the profile of the dopant as it was originally implanted.

5. The method as claimed in claim 1 wherein forming raised source/drain dopant implanted regions further comprises implanting the regions with a dopant selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof.

6. The method as claimed in claim 1 wherein forming silicide layers further comprises depositing a metallic layer selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof.

7. A method of forming a device comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming a sidewall spacer on the semiconductor substrate adjacent the gate and the gate dielectric;

forming a thickening layer by selective epitaxial growth of silicon on the surface of the semiconductor substrate adjacent the sidewall spacer and the gate;

forming raised source/drain dopant implanted regions in at least a portion of the thickening layer and the adjacent top of the semiconductor substrate;

forming silicide layers in at least a portion of the raised source/drain dopant implanted regions to form source/drain regions, beneath the silicide layers, that are enriched with dopant from the silicide layers;

forming a silicide layer on the gate;

depositing a dielectric layer over the silicide layers; and

forming contacts in the dielectric layer to the silicide layers.

8. The method as claimed in claim 7 wherein forming the raised source/drain dopant implanted regions further comprises implanting dopant into the thickening layer and the adjacent top of the semiconductor substrate.

9. The method as claimed in claim 7 wherein forming silicide layers in the raised source/drain dopant implanted regions further comprises:

depositing metallic layers on the raised source/drain dopant implanted regions; and

forming silicide layers by thermal silicidation of the metallic layers into the silicon material of the raised source/drain dopant implanted regions.

10. The method as claimed in claim 7 wherein forming silicide layers in the raised source/drain dopant implanted regions to form source/drain regions therebeneath that are enriched with dopant from the silicide layers further comprises forming source/drain regions that are enriched with a dopant profile that is steeper than the profile of the dopant as it was originally implanted.

11. The method as claimed in claim 7 wherein forming raised source/drain dopant implanted regions further comprises implanting the regions with a dopant selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof.

12. The method as claimed in claim 7 wherein forming silicide layers further comprises depositing a metallic layer selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof.

13. A device comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

a sidewall spacer on the semiconductor substrate adjacent the gate and the gate dielectric;

an epitaxial thickening layer on the semiconductor substrate adjacent the sidewall spacer;

silicide layers in at least a portion of the epitaxial thickening layer;

source/drain regions, beneath the silicide layers, that are enriched with dopant from the silicide layers;

a dielectric layer over the silicide layers; and

contacts in the dielectric layer to the silicide layers.

14. The device as claimed in claim 13 wherein the epitaxial thickening layer and the adjacent top of the semiconductor substrate are dopant implanted regions.

15. The device as claimed in claim 13 wherein the silicide layers in the epitaxial thickening layer further comprise silicide layers formed by thermal silicidation of deposited metallic layers into a dopant implanted epitaxial thickening layer.

16. The device as claimed in claim 13 wherein the source/drain regions that are enriched with dopant from the silicide layers have a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers.

17. The device as claimed in claim 13 wherein the dopant is a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof.

18. The device as claimed in claim 13 wherein the silicide layers are a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof.

19. A device comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

a sidewall spacer on the semiconductor substrate adjacent the gate and the gate dielectric;

an epitaxial silicon thickening layer on the surface of the semiconductor substrate adjacent the sidewall spacer and the gate, the epitaxial thickening layer and the adjacent top of the semiconductor substrate being dopant implanted regions;

silicide layers in at least a portion of the epitaxial silicon thickening layer;

source/drain regions, beneath the silicide layers, that are enriched with dopant, from the silicide layers, that has a dopant profile that is steeper than the profile of dopant lacking enrichment from the silicide layers;

the dopant being a material selected from a group consisting of arsenic, phosphorus, antimony, boron, indium, and a combination thereof;

a silicide layer on the gate;

the silicide layers being a silicide of a metal selected from a group consisting of cobalt, nickel, titanium, hafnium, platinum, and a combination thereof;

a dielectric layer over the silicide layers; and

contacts in the dielectric layer to the silicide layers.

20. The device as claimed in claim 19 wherein the silicide layers in the epitaxial silicon thickening layer further comprise silicide layers formed by thermal silicidation of deposited metallic layers into a dopant implanted epitaxial silicon thickening layer.